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Attorney's Docket No. 4906P114

**SEP 25 2006**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Michael McClary, et al.

Serial No. 10/602,461

Filed: June 23, 2003

For: Repeated Switching of a Cross-  
Connect and a Timing Source in a  
Network Element Through the Use  
of a Phase Adjuster

Examiner: Nitin Patel

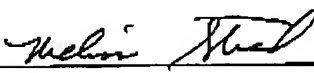
Art Group: 2116

Mail Stop Fee Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**STATEMENT OF ATTESTATION UNDER 37 C.F.R. §1.8 (b)(3)**

I, Melissa Stead, under the penalty of perjury, declare that I personally mailed the  
Amendment and Response to Office Action in the above-mentioned Application on March 22,  
2006 by first-class U.S. mail.

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Melissa Stead

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310 820 5988 SEP 25 2006 P.001/016 F-679

# BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

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## FACSIMILE COVER SHEET

Deliver to: Nitin Patel, USPTO Art Group: 2116  
Facsimile No.: 571-273-8300 Date: September 25, 2006  
From: Jonathan S. Miller, Reg. No. 48,534  
Our Docket No.: 4906P114 Number of pages 16 including this sheet.  
Application No.: 10/602,461 Filing Date: 6/23/2003  
Docket Due Date(s): \_\_\_\_\_

Enclosed are the following documents:

<input type="checkbox"/> Amendment: _____ (____ pgs)	<input type="checkbox"/> Issue Fee Transmittal
<input type="checkbox"/> Appeal Brief (____ pgs)	<input type="checkbox"/> Notice of Appeal
<input type="checkbox"/> Application: _____ (____ pgs) w/cover & abstract)	<input type="checkbox"/> Petition for: _____
<input type="checkbox"/> Assignment & Cover Sheet (____ pgs)	<input type="checkbox"/> Request for Continued Examination (RCE)
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<input type="checkbox"/> Drawings: ____ sheets, ____ figures	<input type="checkbox"/> Response to Notice of Missing Parts & Formalities Letter
<input type="checkbox"/> Extension of Time: _____	<input type="checkbox"/> Response to Written Opinion (____ pgs)
<input type="checkbox"/> Fee Transmittal (in duplicate)	<input type="checkbox"/> Terminal Disclaimer
<input type="checkbox"/> IDS & PTO/SB/08 (____ pgs)	<input type="checkbox"/> Transmittal of Publication Fee Due
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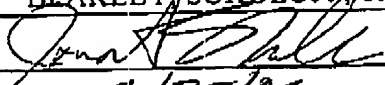
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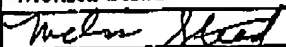
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SEP 25 2006

<b>TRANSMITTAL FORM</b> (to be used for all correspondence after initial filing)		Application No.	10/602,461
		Filing Date	June 23, 2003
		First Named Inventor	
		Art Unit	2116
		Examiner Name	Nitin Patel
Total Number of Pages in This Submission	7	Attorney Docket Number	4906P114

ENCLOSURES (check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Response <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> PTO/SB/08 <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Basic Filing Fee <input type="checkbox"/> Declaration/POA <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px; margin-top: 5px;">         Request for Original Filing Date Under 37 C.F.R. 1.8(b); Statement of Attestation under 37 C.F.R. 1.8(b)(3); Previously filed fee transmittal; Previously filed Amendment and Response to Office Action       </div>
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Jonathan S. Miller, Reg. No. 48,534 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	9/25/06

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SEP 25 2006

<b>FEE TRANSMITTAL for FY 2005</b> <small>Patent fees are subject to annual revision.</small>		Complete If Known	
		Application Number	10/602,461
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27.		Filing Date	June 23, 2003
		First Named Inventor	
<b>TOTAL AMOUNT OF PAYMENT</b> (\$)		Examiner Name	Nitin Patel
		Art Unit	2116
		Attorney Docket No.	4906P114

<b>METHOD OF PAYMENT</b> (check all that apply)	
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<input checked="" type="checkbox"/> Deposit Account Deposit Account Number: <u>02-2666</u> Deposit Account Name: <u>Blakely, Sokoloff, Taylor &amp; Zafman LLP</u>	
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Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451		2451		Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify) _____					
				<b>SUBTOTAL (2)</b>	<b>(\$)</b>

<b>SUBMITTED BY</b>		Complete (if applicable)	
Name (Print/Type)	Jonathan S. Miller	Registration No. (Attorney/Agent)	48,534
Signature		Telephone	(310) 207-3800
		Date	11/25/06

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Attorney's Docket No. 4906P114

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Michael McClary, et al.	)	Examiner: Nitin Patel
	)	
Serial No. 10/602,461	)	Art Group: 2116
	)	
Filed: June 23, 2003	)	
	)	
For: Repeated Switching of a Cross-	)	
Connect and a Timing Source in a	)	
Network Element Through the Use	)	
of a Phase Adjuster	)	

Mail Stop Fee Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

REQUEST FOR ORIGINAL FILING DATE UNDER 37 C.F.R. § 1.8 (b)

This resubmission is to request the original mailing date of the Amendment and Response to Office Action, mailed March 22, 2006 under 37 C.F.R. § 1.8 (b). Enclosed is a copy of the Amendment and Response to Office Action, as filed, including a certificate of mailing. Also enclosed is the fee transmittal that accompanied the response when filed.

A return postcard has not been received and no indication of a receipt of the response was found in the PAIR system. Please find attached a Statement of Attestation under 37 C.F.R. § 1.8(b)(3) from the individual responsible for mailing the above mentioned document and who signed the original certificate of mailing.

Please charge all the appropriate fees to Deposit Account No. 02-2666. A copy of the Fee Transmittal is enclosed for deposit account charging purposes.

If you have any questions please contact me at (310) 500-4767.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 9/25, 2006

  
Jonathan S. Miller Reg. No. 48,534

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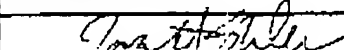
9-25-06  
Date

SEP 25 2006

<b>FEE TRANSMITTAL for FY 2005</b> <small>Patent fees are subject to annual revision.</small>		Complete If Known	
		Application Number	10/602,461
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27.		Filing Date	June 23, 2003
		First Named Inventor	
		Examiner Name	Thomas C. Lee
		Art Unit	2181
TOTAL AMOUNT OF PAYMENT (\$)		Attorney Docket No.	4906P114

<b>METHOD OF PAYMENT</b> (check all that apply)	
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<input checked="" type="checkbox"/> Deposit Account Deposit Account Number: <u>02-2666</u> Deposit Account Name: <u>Blakely, Sokoloff, Taylor &amp; Zafman LLP</u>	
For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)	
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<input checked="" type="checkbox"/> Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. <input type="checkbox"/> Credit any overpayments	

FEE CALCULATION					
Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
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1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify) _____					
				SUBTOTAL (2)	(\$)

SUBMITTED BY		Complete (if applicable)	
Name (Print/Type)	Jonathan S. Miller	Registration No. (Attorney/Agent)	48,534
Signature		Telephone	(310) 207-3800
		Date	3/24/06

Based on PTO/5B/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (w/n) 12/15/2004.  
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PATENT

Attorney's Docket No. 4906P114

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Michael McClary, et al.

Serial No. 10/602,461

Filed: June 23, 2003

For: Repeated Switching of a Cross-  
Connect and a Timing Source in a  
Network Element Through the Use  
of a Phase Adjuster

Examiner: Lee C. Thomas

Art Group: 2115

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Alexandria, VA 22313-1450

**Amendment and Response to Office Action**

In response to the Office Action mailed February 1, 2006, in connection with the above referenced patent application, Applicants respectfully request reconsideration in view of the following amendments and remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of the paper.

# **AMENDMENTS TO THE CLAIMS**

The listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)
2. (Currently Amended) A method comprising:  
storing data from a primary and a secondary source into a primary memory and a secondary memory based on a primary clock signal and a secondary clock signal;  
framing data being outputted from the primary and the secondary memory; and  
adjusting the primary clock signal to adjust [the] an occupancy of the primary memory.
3. (Previously Presented) The method of claim 2, further comprising:  
generating a signal indicating that a phase adjustment of the primary clock signal is needed.
4. (Previously Presented) The method of claim 2, further comprising:  
calibrating a phase adjuster for the primary clock signal.
5. (Previously Presented) The method of claim 2, further comprising:  
calculating a delay for the primary clock signal to adjust the primary clock signal to accelerate or decelerate the framing of data in the primary memory.
6. (Previously Presented) The method of claim 2, wherein the primary memory is a memory that is currently in use for transmitting a frame, and  
wherein the secondary memory is a memory that is not in use for transmitting a frame.
7. (Previously Presented) The method of claim 2, further comprising:

adjusting the primary clock signal to adjust the occupancy of an egress memory.

8. (Currently Amended) A[n] device comprising:

a primary memory;

a secondary memory; and

a clock control logic circuit coupled to the primary memory and secondary memory to

adjust a primary clock signal to synchronize ~~adjust~~ an occupancy of the primary memory and the secondary memory.

9. (Previously Presented) The device of claim 8, further comprising:

a primary deframer coupled to the primary memory; and

a secondary deframer coupled to the secondary memory.

10. (Previously Presented) The device of claim 8, wherein the clock control logic comprises:

a phase adjuster;

cycle control logic coupled to the phase adjuster; and

step pulse generator logic coupled to the cycle control logic.

11. (Currently Amended) The device of claim [8]10, wherein the phase adjuster comprises:

a set of delay cells to alter the phase of a primary clock signal.

12. (Currently Amended) An apparatus comprising:

a primary control card;

a secondary control card; and

a traffic card coupled to the primary control card and secondary control card, the traffic card having a clock control logic circuit coupled to a primary memory and secondary memory to

adjust a primary clock signal to ~~adjust~~ synchronize the an occupancy of the primary memory and the secondary memory.

13. (Previously Presented) The apparatus of claim 12, wherein the primary control card is in use and the secondary control card is a back up card.

14. (Previously Presented) The device of claim 12, further comprising:  
a second traffic card coupled to the primary control card and the secondary control card.

15. (Previously Presented) The device of claim 12, wherein the clock control logic comprises:

a phase adjuster;  
cycle control logic coupled to the phase adjuster; and  
step pulse generator logic coupled to the cycle control logic.

16. (Previously Presented) An apparatus comprising:  
means for storing data from a primary and a secondary source into a primary memory and a secondary memory based on a primary clock signal and a secondary clock signal;  
means for framing data being outputted from the primary and the secondary memory; and  
means for adjusting the primary clock signal to adjust an occupancy of the primary memory.

17. (Previously Presented) The apparatus of claim 16, further comprising:  
means for generating a signal indicating that a phase adjustment of the primary clock signal is needed.

18. (Previously Presented) The apparatus of claim 16, further comprising:  
means for calibrating a phase adjuster for the primary clock signal.

19. (Previously Presented) The method of claim 16, further comprising:  
means for calculating a delay for the primary clock signal to adjust the primary clock signal to accelerate or decelerate the framing of data in the primary memory.
20. (Previously Presented) The method of 16, further comprising:  
means for adjusting the primary clock signal to adjust an occupancy of an egress memory.
21. (Previously Presented) A machine readable medium, having instruction stored therein, which when executed cause a computer to perform a set of operations comprising:  
storing data from a primary and a secondary source into a primary memory and a secondary memory based on a primary clock signal and a secondary clock signal;  
framing data being outputted from the primary and the secondary memory; and  
adjusting the primary clock signal to adjust an occupancy of the primary memory.
22. (Previously Presented) The machine readable medium of claim 21, having further instructions stored therein, which when executed cause a computer to perform a set of operations comprising:  
generating a signal indicating that a phase adjustment of the primary clock signal is needed.
23. (Previously Presented) The machine readable medium of claim 21, having further instructions stored therein, which when executed cause a computer to perform a set of operations comprising:  
calibrating a phase adjuster for the primary clock signal.

24. (Previously Presented) The machine readable medium of claim 21, having further instructions stored therein, which when executed cause a computer to perform a set of operations comprising:

calculating the delay for the primary clock signal to adjust the primary clock signal to accelerate or decelerate the framing of data in the primary memory.

25. (Previously Presented) The machine readable medium of claim 21, wherein the primary memory is a memory that is currently in use for transmitting a frame, and

wherein the secondary memory is a memory that is not in use for transmitting a frame.

26. (New) An apparatus comprising:

a traffic card including,

a first and second ingress FIFO to be coupled to respectively receive both data and a clock signal from a first and second control card;

a first and second deframer respectively coupled to said first and second ingress FIFOs;

an aligner coupled to said first and second FIFO to keep the occupancy of data therein in sync based upon detected differences in alignment of data being received by the first and second deframers;

a clock control logic to receive the clock signal from each of said first and second control cards, to exchange with a PLL a first clock signal for a PLL adjusted clock signal, and to provide said PLL adjusted clock signal to said aligner, said first ingress FIFO, and said second ingress FIFO, said clock control logic including,

a phrase adjuster to provide said first clock signal based on a currently selected one of the clock signals from said first and second control cards.

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REMARKS

In response to the above identified Office Action, the applicants amend claims 2, 8, 11 and 12. The applicants add claim 26. No claims have been canceled. Accordingly, claims 2-26 are pending in the application.

I. Objections to the Specification

The Examiner has objected to the title of the application, stating that the title of the invention is not descriptive. The applicants believe that the title describes an embodiment of the invention presented in the application. The applicants request clarification as to what aspects of the invention must be described by the title. Accordingly, reconsideration and withdrawal of the objection to the title is requested.

II. Objections to the Claims

The Examiner has objected to claims 2, 8 and 12 stating that these claims include informalities. The applicants have amended each of these claims to correct the informalities noted by the Examiner. Accordingly, reconsideration and withdrawal of the objection to these claims are requested.

III. Claims Rejected Under 35 U.S.C. § 112, second paragraph

Claim 11 has been rejected under 35 U.S.C. § 112, second paragraph, for including a limitation without proper antecedent basis. The applicants have amended claim 11 to depend from claim 10 to provide proper antecedent basis for "the phase adjuster." Accordingly, reconsideration and withdrawal of the indefiniteness rejection of claim 11 are requested.

IV. Claims Provisionally Rejected on the Ground of Non-Statutory Obviousness Type Double Patenting

The Examiner has rejected claims 2-25, provisionally, as being unpatentable over claims 1-25 of copending Application No. 10/402,481. The applicants hold in abeyance any response to this provisional double patenting rejection until such time as it becomes non-provisional.

V. Claims Rejected Under 35 U.S.C. § 102

Claims 8 and 12 stand rejected under 35 U.S.C. § 102, as being anticipated by U.S. Patent No. 6,982,993 issued to Claveloux et al (hereinafter "Claveloux").

To establish anticipation, the Examiner must show that a single reference teaches each of the elements of a claim. Claims 8 and 12, as amended, include the elements of "a clock control logic circuit coupled to the primary memory and secondary memory to adjust a primary clock signal to synchronize an occupancy of the primary memory and the secondary memory." The applicants have reviewed Claveloux, but have been unable to discern any part therein that teaches these elements of claims 8 and 12. Accordingly, reconsideration and withdrawal of the anticipation rejection of claims 8 and 12 are requested.

VI. Allowable Subject Matter

The Examiner has not set forth any basis for rejecting claims 2-7, 9-11 and 13-25 other than the provisional double patenting rejection. Thus, the applicants note with appreciation that the Examiner implies that these claims contain allowable subject matter. Because the only basis of rejection is provision, applicants believe that these claims are in condition for allowance.

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CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 2-26, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 3/22, 2006

Jonathan S. Miller  
Jonathan S. Miller, Reg. No. 48,534

12400 Wilshire Blvd.  
Seventh Floor  
Los Angeles, California 90025  
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Melissa Stead